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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/390,079	09/03/1999	DARREN KERR	112025-0167	6305

7590 02/28/2006

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	09/390,079	KERR ET AL.	
	Examiner	Art Unit	
	Richard Ellis	2183	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 January 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires ______months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *None*.
   Claim(s) objected to: *None*.
   Claim(s) rejected: *67-117*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheets (3 pages) for explanations.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____
13. ☐ Other: _____.

Richard Ellis

RICHARD L. ELLIS
PRIMARY EXAMINER

Applicant argues that:

> "Operation of the design of Fig. 1 of Hao appears to use the output of register 5 and register 6 to control the switches indicated as "A", "B", and "C" of Hao's ALU 2 "22", and therefore for registers 5 and 6 of ALU 1 to control the inputs to ALU 2. ...
>
> By the horizontal line from register 5 output, input to ALU 2 at both input "A" from register 25 and input to input "B" from register 26 may be controlled by register 5.
>
> By the lower horizontal line from register 6 output to the input "C" of ALU 2 "22", control is indicated, but there is no signal input line to input "C". Therefore, the best guess is that input "C" of ALU 2 "22" simply disables ALU 2 "22", as described by Hao at his Col. 9 lines 61 through Col. 10 line 4) which state in relevant part:
>
> 'As the STAGING CYCLE begins, control calls for "Access source regs for OP1" which accesses OP1 information from GPR's 4 in FIG. 1. Data is set into the staging registers S1 and S2 (5,6 in Fig. 1). In the appropriate situation (a Store instruction) store data is accessed from GPR's 24 (FIG. 1) for the secondary data flow. ...' "

Applicant, however, is factually incorrect in this argument. First, applicant argues that the horizontal lines in Fig. 1 connecting staging registers 5,6 to ALU2 (22) are <u>control</u> lines. This argument is not factually incorrect based upon the teachings of Hao. Fig. 1 is clearly labeled "**<u>Data</u>** Flow" (see label below "FIG. 1" in lower right corner). Hao additionally describes the figure at col. 5 lines 27-30 as showing the **<u>data</u>** flow" "FIG. 1 is a schematic diagram showing **<u>data</u>** flow through the pipelined processor, ..." (emphasis added) and at col. 6 lines 20-22: "An overview of the pipelined processor **<u>data</u>** flows is shown in FIG. 1." (emphasis added). This clearly indicates that Hao intended for fig. 1 to represent the paths to which data moves (or flows) around the pipeline processor.

Second, applicant argues that the lower horizontal line to input C of ALU2 is further a control line and then guesses that this line simply disables ALU2. Applicant is also factually incorrect in this argument. Initially, applicant's quotation of Hao's col. 9 line 60 to col. 10 line 4 does not support applicants incorrect guess that the horizontal line between element 6 and input C is control that disables ALU2. The quotation states that in the situation of a store instruction, store data is accessed from GPR's 24. It says nothing at all about the line to input C of ALU2.

Furthermore, the specific disclosed purpose of Hao's system is to allow two otherwise dependent operations that would normally require sequential execution to be

performed in parallel. Hao shows a specific example of this situation at col. 7 lines 50-67, reproduced below:

> If the first instruction is an ADD REGISTER, and the second instruction is dependent upon the result, then ALU1's operation can be duplicated in two of the three ports of ALU2, and when possible combined with another operand from the second instruction, and executed concurrently with the first instruction. This is concurrent instruction execution of a greater complexity, where the second instruction is dependent on replication of the completion of the first instruction.
>
> Examples where simultaneous execution is allowed:
>
> Ex. 1 Two dependent adds
> inst 1 R3 ← R1 + R2
> inst 2 R5 ← R3 + R4
> ALU1 (Inst 1) adder (2 FIG. 1) R1 + R2
> ALU2 (Inst 2) adder (22 FIG. 1) R1 + R2 + R4
> (Overcomes Data Dependency)

As seen from the above text of Hao, ALU2 is performing an addition of three operands, R1, R2, and R4. However, as seen from fig. 1, ALU2 has only two inputs to GPR's 24 and two staging registers 25, 26. In order to present three operands to the three inputs of ALU2, two of the operands (R1, R2, the two operands in common between the two ALU's) are sent to ALU2 via the two horizontal lines to inputs A and C of ALU2. Then, the third operand (R4) is accessed from GPR 24 and staging register 26 into input B of ALU2, resulting in ALU2 having available all three operands (R1, R2, and R4) with which to calculate their sum.

This method of operation is clearly described by Hao in fig. 4C. In fig. 4C, there is found this test: "source 2 of op2 is sink of op1?". This corresponds to R3 in Ex. 1 quoted above, where source2 (R3 in Ex. 1 on inst2 line) of op2 (inst 2 in Ex. 1) is the sink (R3 in Ex. 1 on inst 1 line) of op1 (inst 1 in Ex. 1). Next, the system checks to determine if op2 is valid, and if so, then the step that is followed is: "gate alu1 staging regs to adder2 via ports A and C (21)".

In order to "gate" the "alu1 staging regs" to "adder2" via "ports A and C", the data from the alu1 staging registers (5, 6 in fig. 1) must flow across the horizontal lines connecting registers 5 and 6 to ALU2 inputs A and C, and as such, the lines on the figure must be **data** lines and not control lines.

Therefore, as shown by this portion of fig. 4C, Hao et al. does indeed teach a multiplexer (shown above input A of ALU2) which has a first input coupled to a first input of a first

ALU (the cited horizontal line connecting the input A mux to the left input of ALU1 and staging register 5), a second input coupled to a first input register of the second ALU (the cited line from the input A mux to staging register 26, and an output directly providing a first input to the second ALU (the cited connection of the mux directly to the input A of ALU2), the mux permitting both the first and second alu (ALU2, ALU2) to share the source operand stored in the first input register (5) of the first ALU (ALU1) as claimed by applicant. The horizontal lines are what allow "gat[ing the] alu1 staging regs (5,6) to adder2 via ports A and C (21)", and by gating staging register 5 to adder2 port A, port A shares the same input value with the left input of ALU1.